SECTION 4
SWITCHED CAPACITOR VOLTAGE CONVERTERS

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INTRODUCTION

In the previous section, we saw how inductors can be used to transfer energy and perform voltage conversions. This section examines switched capacitor voltage converters which accomplish energy transfer and voltage conversion using capacitors.

The two most common switched capacitor voltage converters are the *voltage inverter* and the *voltage doubler* circuit shown in Figure 4.1. In the voltage inverter, the charge pump capacitor, C1, is charged to the input voltage during the first half of the switching cycle. During the second half of the switching cycle, its voltage is inverted and applied to capacitor C2 and the load. The output voltage is the negative of the input voltage, and the average input current is approximately equal to the output current. The switching frequency impacts the size of the external capacitors required, and higher switching frequencies allow the use of smaller capacitors. The duty cycle - defined as the ratio of charging time for C1 to the entire switching cycle time - is usually 50%, because that generally yields the optimal charge transfer efficiency.

After initial start-up transient conditions and when a steady-state condition is reached, the charge pump capacitor only has to supply a small amount of charge to the output capacitor on each switching cycle. The amount of charge transferred depends upon the load current and the switching frequency. During the time the pump capacitor is charged by the input voltage, the output capacitor C2 must supply the load current. The load current flowing out of C2 causes a droop in the output voltage which corresponds to a component of output voltage ripple. Higher switching frequencies allow smaller capacitors for the same amount of droop. There are, however, practical limitations on the switching speeds and switching losses, and switching frequencies are generally limited to a few hundred kHz.

The voltage doubler works similarly to the inverter; however, the pump capacitor is placed in series with the input voltage during its discharge cycle, thereby accomplishing the voltage doubling function. In the voltage doubler, the average input current is approximately twice the average output current.

The basic inverter and doubler circuits provide no output voltage regulation, however, techniques exist to add regulated capability and have been implemented in the ADP3603/3604/3605/3607.

BASIC SWITCHED CAPACITOR VOLTAGE INVERTER AND VOLTAGE DOUBLER

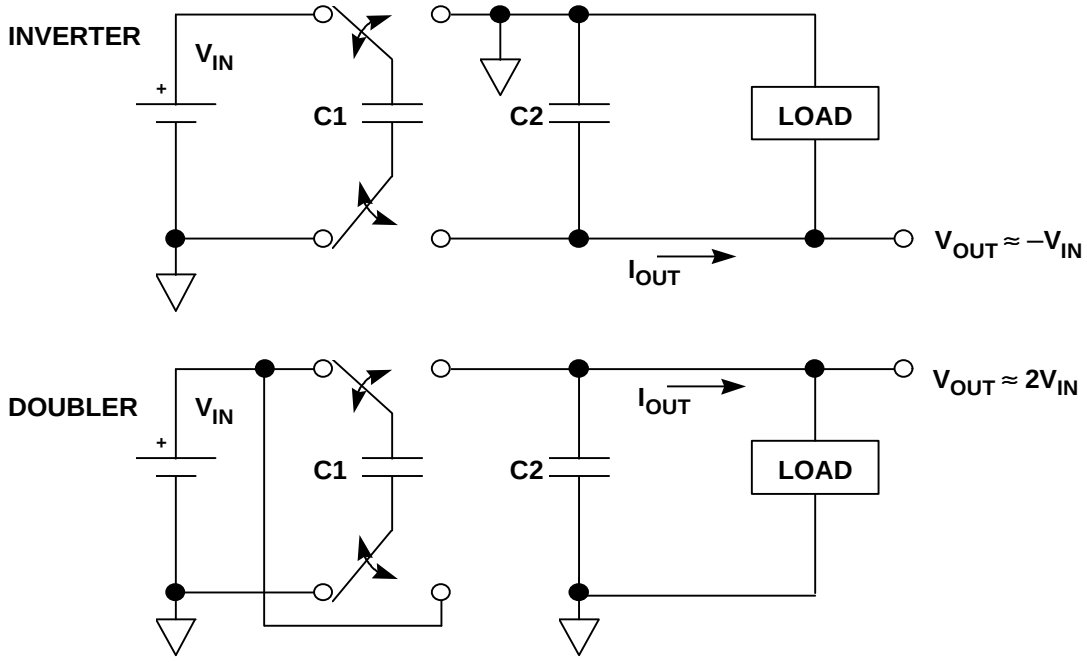


Figure 4.1

There are certain advantages and disadvantages of using switched capacitor techniques rather than inductor-based switching regulators. An obvious key advantage is the elimination of the inductor and the related magnetic design issues. In addition, these converters typically have relatively low noise and minimal radiated EMI. Application circuits are simple, and usually only two or three external capacitors are required. Because there is no need for an inductor, the final PCB component height can generally be made smaller than a comparable switching regulator. This is important in many applications such as display panels.

Switched capacitor inverters are low cost and compact and are capable of achieving efficiencies greater than 90%. Obviously, the current output is limited by the size of the capacitors and the current carrying capacity of the switches. Typical IC switched capacitor inverters have maximum output currents of about 150mA maximum.

Switched capacitor voltage converters do not maintain high efficiency for a wide range of ratios of input to output voltages, unlike their switching regulator counterparts. Because the input to output current ratio is scaled according to the basic voltage conversion (i.e., doubled for a doubler, inverted for an inverter) regardless of whether or not regulation is used to reduce the doubled or inverted voltage, any output voltage magnitude less than $2V_{IN}$ for a doubler or less than $|V_{IN}|$ for an inverter will result in additional power dissipation within the converter, and efficiency will be degraded proportionally.

SWITCHED CAPACITOR VOLTAGE CONVERTERS

- **No Inductors!**
- **Minimal Radiated EMI**
- **Simple Implementation: Only 2 External Capacitors (Plus an Input Capacitor if Required)**
- **Efficiency > 90% Achievable**
- **Optimized for Doubling or Inverting Supply Voltage - Efficiency Degrades for Other Output Voltages**
- **Low Cost, Compact, Low Profile (Height)**

- **Parts with Voltage Regulation are Available:**

  ADP3603/ADP3604/ADP3605/ADP3607

Figure 4.2

The voltage inverter is useful where a relatively low current negative voltage is required in addition to the primary positive voltage. This may occur in a single supply system where only a few high performance parts require the negative voltage. Similarly, voltage doublers are useful in low current applications where a voltage greater than the primary supply voltage is required.

CHARGE TRANSFER USING CAPACITORS

A fundamental understanding of capacitors (theoretical and real) is required in order to master the subtleties of switched capacitor voltage converters. Figure 4.3 shows the theoretical capacitor and its real-world counterpart. If the capacitor is charged to a voltage V, then the total charge stored in the capacitor, q, is given by q = CV. Real capacitors have equivalent series resistance (ESR) and inductance (ESL) as shown in the diagram, but these parasitics do not affect the ability of the capacitor to store charge. They can, however, have a large effect on the overall efficiency of the switched capacitor voltage converter.

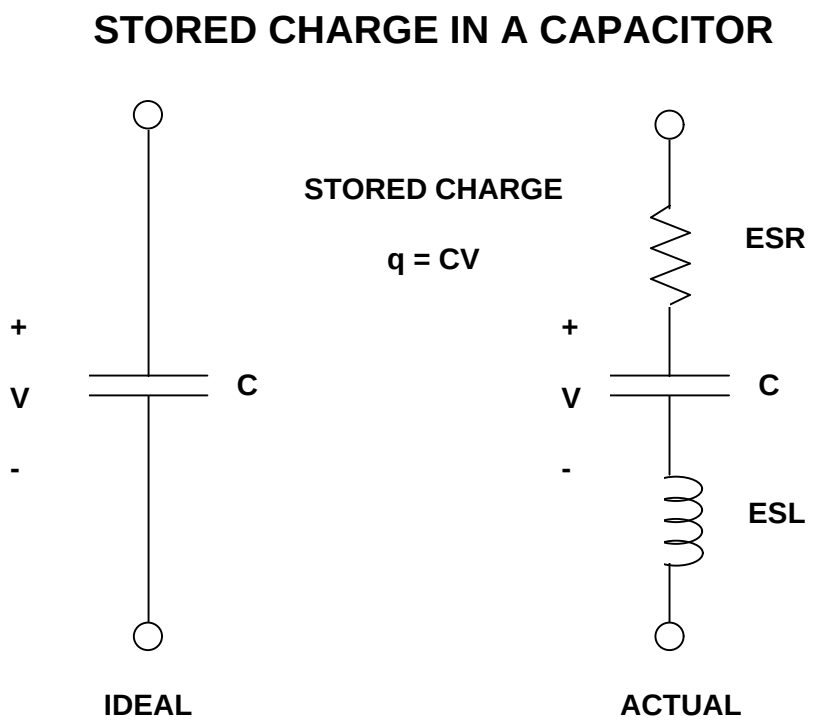


Figure 4.3

If an ideal capacitor is charged with an ideal voltage source as shown in Figure 4.4(A), the capacitor charge buildup occurs instantaneously, corresponding to a unit impulse of current. A practical circuit (Figure 4.4 (B)) will have resistance in the switch (R_{SW}) as well as the equivalent series resistance (ESR) of the capacitor. In addition, the capacitor has an equivalent series inductance (ESL). The charging current path also has an effective series inductance which can be minimized with proper component layout techniques. These parasitics serve to limit the peak current, and also increase the charge transfer time as shown in the diagram. Typical switch resistances can range from 1Ω to 50Ω, and ESRs between 50mΩ and 200mΩ. Typical capacitor values may range from about 0.1µF to 10µF, and typical ESL values 1 to 5nH. Although the equivalent RLC circuit of the capacitor can be underdamped or overdamped, the relatively large switch resistance generally makes the final output voltage response overdamped.

CHARGING A CAPACITOR FROM A VOLTAGE SOURCE

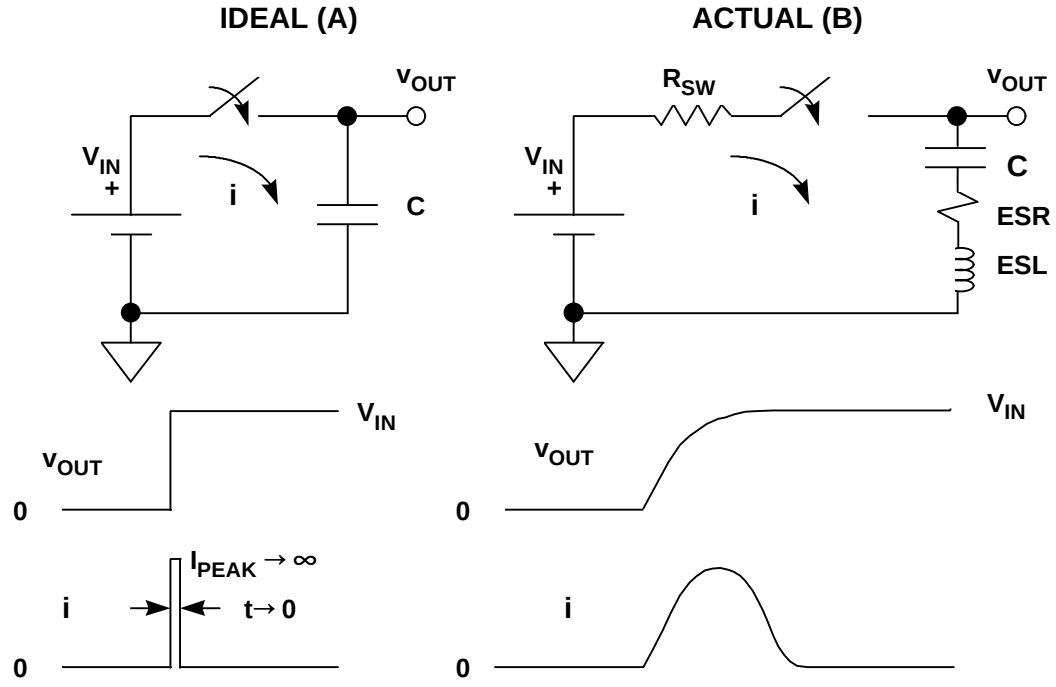


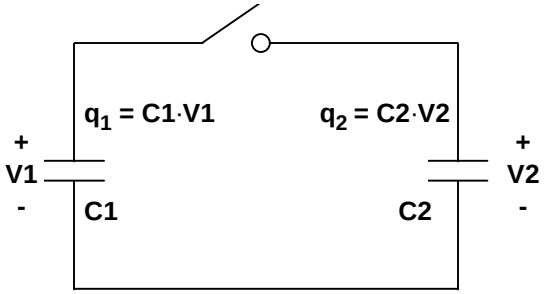
Figure 4.4

The law of conservation of charge states that if two capacitors are connected together, the total charge on the parallel combination is equal to the sum of the original charges on the capacitors. Figure 4.5 shows two capacitors, C1 and C2, each charged to voltages V1 and V2, respectively. When the switch is closed, an impulse of current flows, and the charge is redistributed. The total charge on the parallel combination of the two capacitors is $q_T = C1 \cdot V1 + C2 \cdot V2$. This charge is distributed between the two capacitors, so the new voltage, V_T, across the parallel combination is equal to qT/(C1 + C2), or

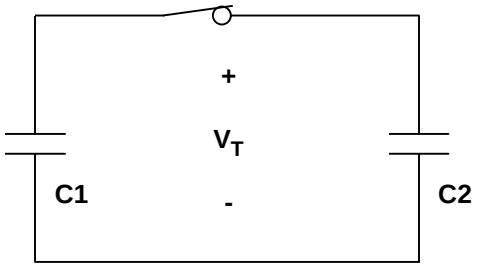
$$V_T = \frac{q_T}{C1 + C2} = \frac{C1 \cdot V1 + C2 \cdot V2}{C1 + C2} = \left(\frac{C1}{C1 + C2}\right)V1 + \left(\frac{C2}{C1 + C2}\right)V2 .$$

This principle may be used in the simple charge pump circuit shown in Figure 4.6. Note that this circuit is neither a doubler nor inverter, but only a voltage replicator. The pump capacitor is C1, and the initial charge on C2 is zero. The pump capacitor is initially charged to V_{IN}. When it is connected to C2, the charge is redistributed, and the output voltage is $V_{IN}/2$ (assuming C1 = C2). On the second transfer cycle, the output voltage is pumped to $V_{IN}/2 + V_{IN}/4$. On the third transfer cycle, the output voltage is pumped to $V_{IN}/2 + V_{IN}/4 + V_{IN}/8$. The waveform shows how the output voltage exponentially approaches V_{IN}.

CHARGE REDISTRIBUTION BETWEEN CAPACITORS



CONSERVATION OF CHARGE:



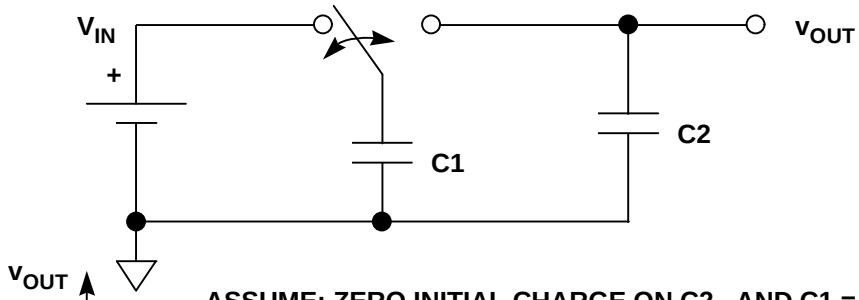
$$q_T = C1 \cdot V1 + C2 \cdot V2$$

$$V_T = \frac{q_T}{C1 + C2}$$

$$V_T = \frac{C1}{C1 + C2} \cdot V1 + \frac{C2}{C1 + C2} \cdot V2$$

Figure 4.5

CONTINUOUS SWITCHING



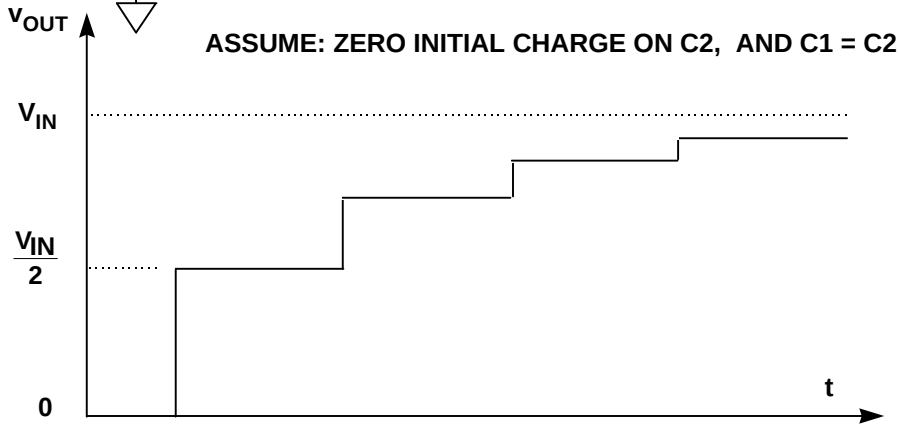


Figure 4.6

Figure 4.7 shows a pump capacitor, C1, switched continuously between the source, V1, and C2 in parallel with the load. The conditions shown are after a steady state condition has been reached. The charge transferred each cycle is $\Delta q = C1(V1 - V2)$. This charge is transferred at the switching frequency, f. This corresponds to an average current (current = charge transferred per unit time) of

$$I = f\,\Delta q = f \cdot C1(V1 - V2), \text{ or}$$

$$I = \frac{V1 - V2}{1/f \cdot C1} .$$

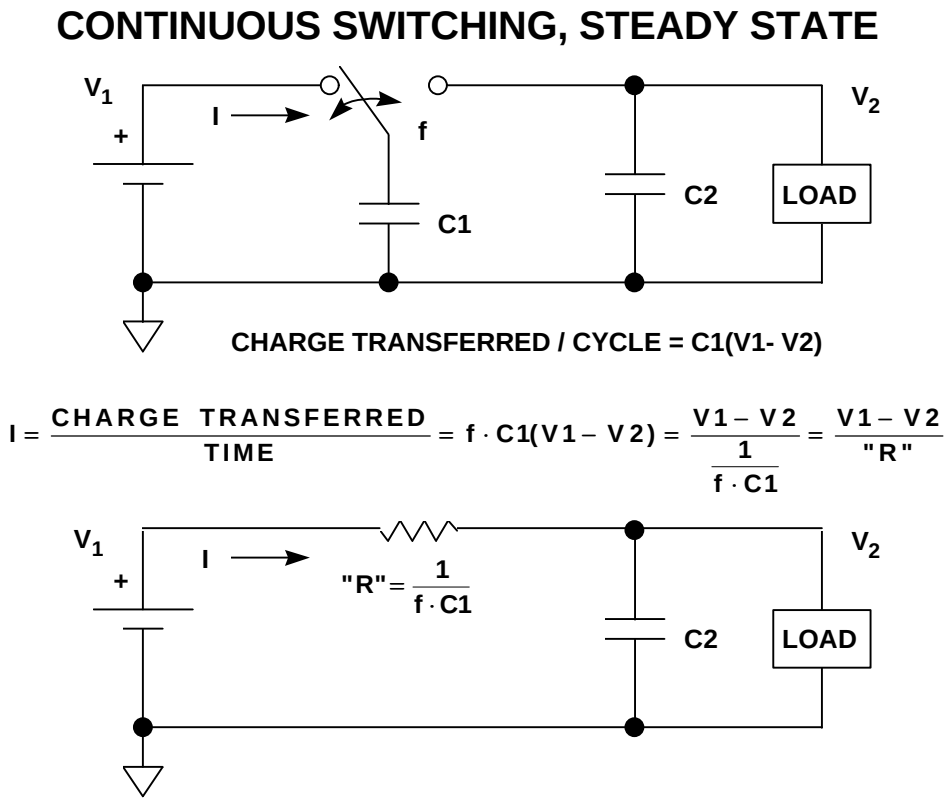


Figure 4.7

Notice that the quantity, 1/f·C1, can be considered an equivalent resistance, "R", connected between the source and the load. The power dissipation associated with this virtual resistance, "R", is essentially forced to be dissipated in the switch on resistance and the capacitor ESR, regardless of how low those values are reduced. (It should be noted that capacitor ESR and the switch on-resistance cause additional power losses as will be discussed shortly.)

In a typical switched capacitor voltage inverter, a capacitance of 10µF switched at 100kHz corresponds to "R" = 1Ω. Obviously, minimizing "R" by increasing the frequency minimizes power loss in the circuit. However, increasing switching frequency tends to increase switching losses. The optimum switched capacitor operating frequency is therefore highly process and device dependent. Therefore, specific recommendations are given in the data sheet for each device.

UNREGULATED SWITCHED CAPACITOR INVERTER AND DOUBLER IMPLEMENTATIONS

An unregulated switched capacitor inverter implementation is shown in Figure 4.8. Notice that the SPDT switches (shown in previous diagrams) actually comprise two SPST switches. The control circuit consists of an oscillator and the switch drive signal generators. Most IC switched capacitor inverters and doublers contain all the control circuits as well as the switches and the oscillator. The pump capacitor, C1, and the load capacitor, C2, are external. Not shown in the diagram is a capacitor on the input which is generally required to ensure low source impedance at the frequencies contained in the switching transients.

The switches used in IC switched capacitor voltage converters may be CMOS or bipolar as shown in Figure 4.9. Standard CMOS processes allow low on-resistance MOSFET switches to be fabricated along with the oscillator and other necessary control circuits. Bipolar processes can also be used, but add cost and increase power dissipation.

SWITCHED CAPACITOR VOLTAGE INVERTER IMPLEMENTATION

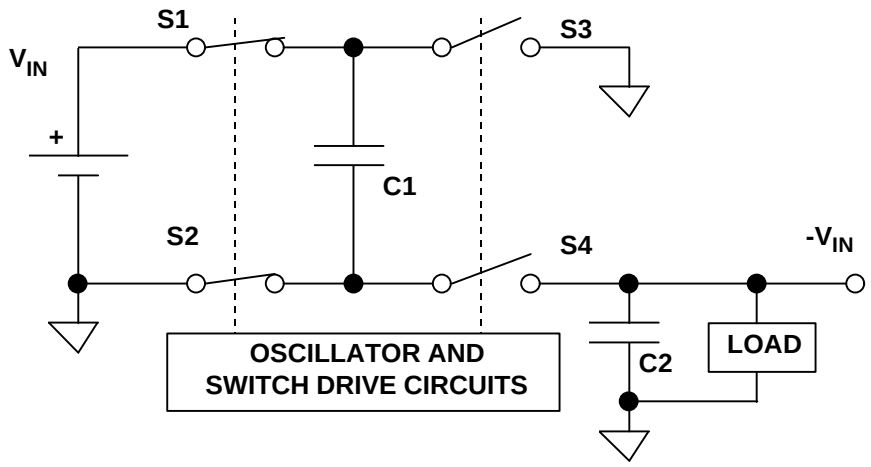


Figure 4.8

SWITCHES USED IN VOLTAGE CONVERTERS

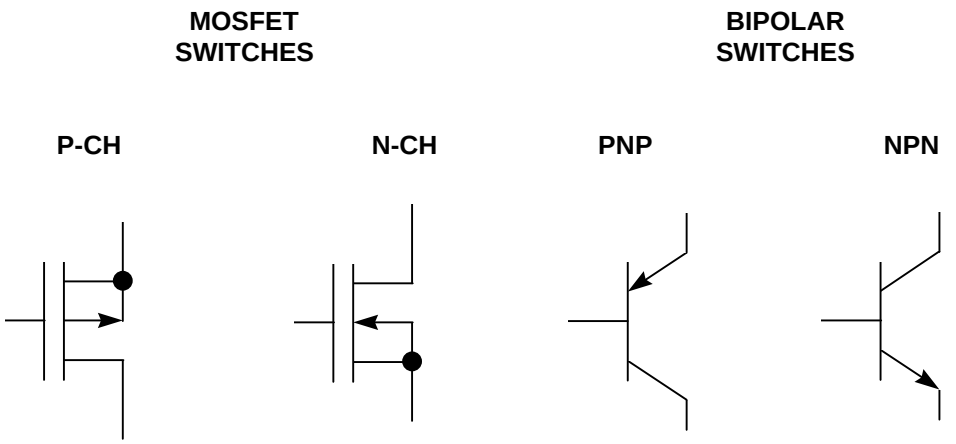


Figure 4.9

VOLTAGE INVERTER AND DOUBLER DYNAMIC OPERATION

The steady-state current and voltage waveforms for a switched capacitor voltage inverter are shown in Figure 4.10. The average value of the input current waveform (A) must be equal to I_{OUT}. When the pump capacitor is connected to the input, a charging current flows. The initial value of this charging current depends on the initial voltage across C1, the ESR of C1, and the resistance of the switches. The switching frequency, switch resistance, and the capacitor ESRs generally limit the peak amplitude of the charging current to less than $2.5I_{OUT}$. The charging current then decays exponentially as C1 is charged. The waveforms in Figure 4.10 assume that the time constant due to capacitor C1, the switch resistance, and the ESR of C1 is several times greater than the switching period (1/f). Smaller time constants will cause the peak currents to increase as well as increase the slopes of the charge/discharge waveforms. Long time constants cause longer start-up times and require larger and more costly capacitors. For the conditions shown in Figure 4.10 (A), the peak value of the input current is only slightly greater than $2I_{OUT}$.

The output current waveform of C1 is shown in Figure 4.10 (B). When C1 is connected to the output capacitor, the step change in the output capacitor current is approximately $2I_{OUT}$. This current step therefore creates an output voltage step equal to $2I_{OUT} \times ESR_{C2}$ as shown in Figure 4.10(C). After the step change, C2 charges linearly by an amount equal to $I_{OUT}/2f \bullet C2$. When C1 is connected back to the input, the ripple waveform reverses direction as shown in the diagram. The total peak-to-peak output ripple voltage is therefore:

$$V_{RIPPLE} \approx 2I_{OUT} \cdot ESR_{C2} + \frac{I_{OUT}}{2f \cdot C2}.$$

VOLTAGE INVERTER WAVEFORMS

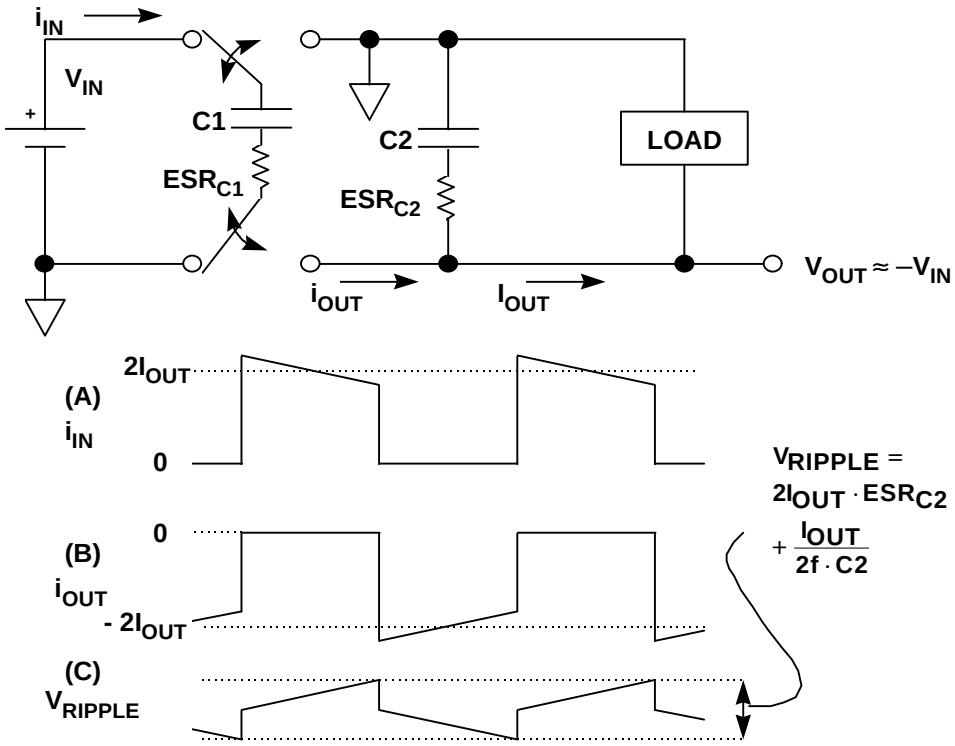


Figure 4.10

VOLTAGE DOUBLER WAVEFORMS

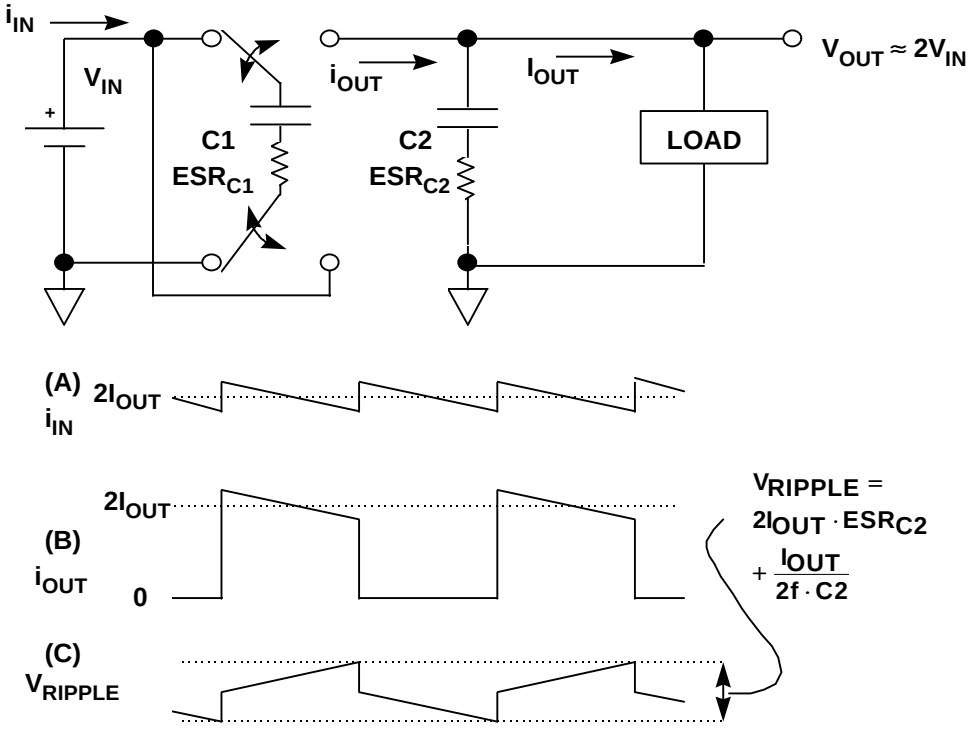


Figure 4.11

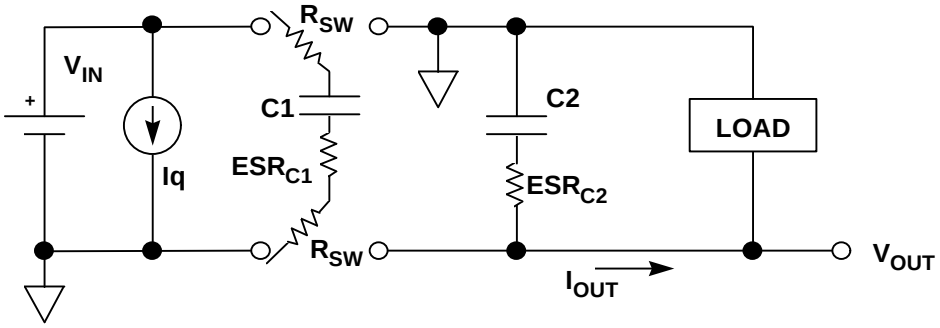
The current and voltage waveforms for a simple voltage doubler are shown in Figure 4.11 and are similar to those of the inverter. Typical voltage ripple for practical switched capacitor voltage inverter/doublers range from 25mV to 100mV, but can be reduced by filtering techniques as described in Section 8 of this book.

Note that the input current waveform has an average value of $2I_{OUT}$ because V_{IN} is connected to C1 during C1's charge cycle and to the load during C1's discharge cycle. The expression for the ripple voltage is identical to that of the voltage inverter.

SWITCHED CAPACITOR VOLTAGE CONVERTER POWER LOSSES

The various sources of power loss in a switched capacitor voltage inverter are shown in Figure 4.12. In addition to the inherent switched capacitor resistance, "R" = 1/f·C1, there are resistances associated with each switch, as well as the ESRs of the capacitors. The quiescent power dissipation, $I_q \cdot V_{IN}$, must also be included, where I_q is the quiescent current drawn by the IC itself.

VOLTAGE INVERTER POWER LOSSES



$$P_{LOSS} = I_{OUT}(V_{IN} - |V_{OUT}|) + I_q V_{IN}$$
$$= I_{OUT}^2 \cdot R_{OUT} + I_q V_{IN}$$

$$R_{OUT} \approx 8R_{SW} + 4ESR_{C1} + \frac{1}{f \cdot C1} + ESR_{C2}$$

Figure 4.12

The power dissipated in the switching arm is first calculated. When C1 is connected to V_{IN}, a current of $2I_{OUT}$ flows through the switch resistances ($2R_{SW}$) and the ESR of C1, ESR_{C1}. When C1 is connected to the output, a current of $2I_{OUT}$ continues to flow through C1, $2R_{SW}$, and ESR_{C1}. Therefore, there is always an rms current of $2I_{OUT}$ flowing through these resistances, resulting in a power dissipation in the switching arm of:

$$P_{SW} = (2I_{OUT})^2 \times (2R_{SW} + ESR_{C1}) = I_{OUT}^2 \times (8R_{SW} + 4ESR_{C1}).$$

In addition to these purely resistive losses, an rms current of I_{OUT} flows through the "resistance" of the switched capacitor, C1, yielding an additional loss of:

$$"P_{C1}" = I_{OUT}^2 \times "R_{C1}" = I_{OUT}^2 \times \frac{1}{f \cdot C1}.$$

The rms current flowing through ESR_{C2} is I_{OUT}, yielding a power dissipation of:

$$P_{ESR_{C2}} = I_{OUT}^2 \times ESR_{C2}.$$

Adding all the resistive power dissipations to the quiescent power dissipation yields:

$$P_{LOSS} = I_{OUT}^2 \times \left(8R_{SW} + 4ESR_{C1} + ESR_{C2} + \frac{1}{f \cdot C1}\right) + IqV_{IN}.$$

All of the resistive losses can be grouped into an equivalent R_{OUT} as shown in the diagram.

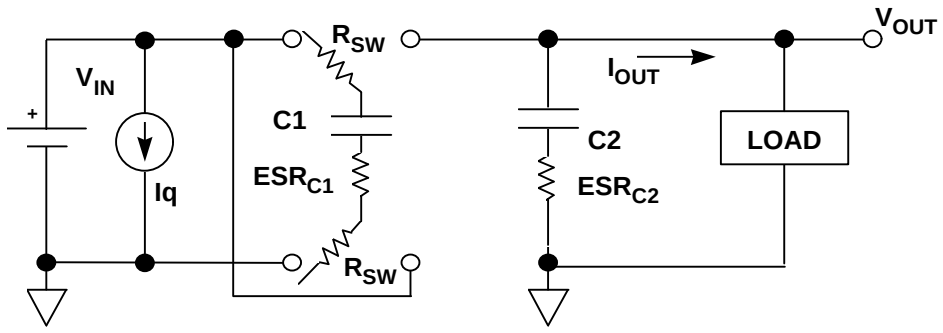
$$R_{OUT} \approx 8R_{SW} + 4ESR_{C1} + 1/f{\cdot}C1 + ESR_{C2}.$$

Typical values for switch resistances are between 1 - 20Ω, and ESRs between 50 and 200mΩ. The values of C1 and f are generally chosen such that the term, 1/f·C1, is less than 1Ω. For instance, 10µF @ 100kHz yields "R" = 1Ω. The dominant sources of power loss in most inverters are therefore the switch resistances and the ESRs of the pump capacitor and output capacitor.

The ADP3603/3604/3605/3607 series regulators have a shutdown control pin which can be asserted when load current is not required. When activated, the shutdown feature reduces quiescent current to a few tens of microamperes.

Power losses in a voltage doubler circuit are shown in Figure 4.13, and the analysis is similar to that of the inverter.

VOLTAGE DOUBLER POWER LOSSES



$$P_{LOSS} = I_{OUT}(2V_{IN} - V_{OUT}) + I_q V_{IN}$$
$$= I_{OUT}^2 \cdot R_{OUT} + I_q V_{IN}$$

$$R_{OUT} \approx 8R_{SW} + 4ESR_{C1} + \frac{1}{f \cdot C1} + ESR_{C2}$$

Figure 4.13

UNREGULATED INVERTER/DOUBLER DESIGN EXAMPLE

The ADM660 is a popular switched capacitor voltage inverter/doubler IC (see Figure 4.14). Switching frequency is selectable (25kHz/120kHz) using the FC input. When the FC input is open, the switching frequency is 25kHz. When it is connected to V+, the frequency increases to 120kHz. Only two external electrolytic capacitors (ESR should be less than 200mΩ) are required for operation (see Figure 4.14). The choice of the value of these capacitors is somewhat flexible. For a 25kHz switching frequency 10µF is recommended, and for 120kHz operation 2.2µF provides comparable performance.

If frequencies less than the selected output frequency are desired, an external capacitor can be placed between the OSC input and ground. The internal oscillator can also be overridden by driving the OSC input with an external logic signal, in which case the internal charge pump frequency is one-half the external clock frequency.

The ADM8660 is similar to the ADM660, however it is optimized for inverter operation and includes a "shutdown" feature which reduces the quiescent current to 5µA. Shutdown recovery time is 500µs. Key specifications for the ADM660/ADM8660 series are given in Figure 4.15.

Efficiency for the ADM660/ADM8660 is greater than 90% for output currents up to 50mA and greater than 80% for output currents to 100mA (see Figure 4.16).

ADM660 SWITCHED CAPACITOR VOLTAGE CONVERTER

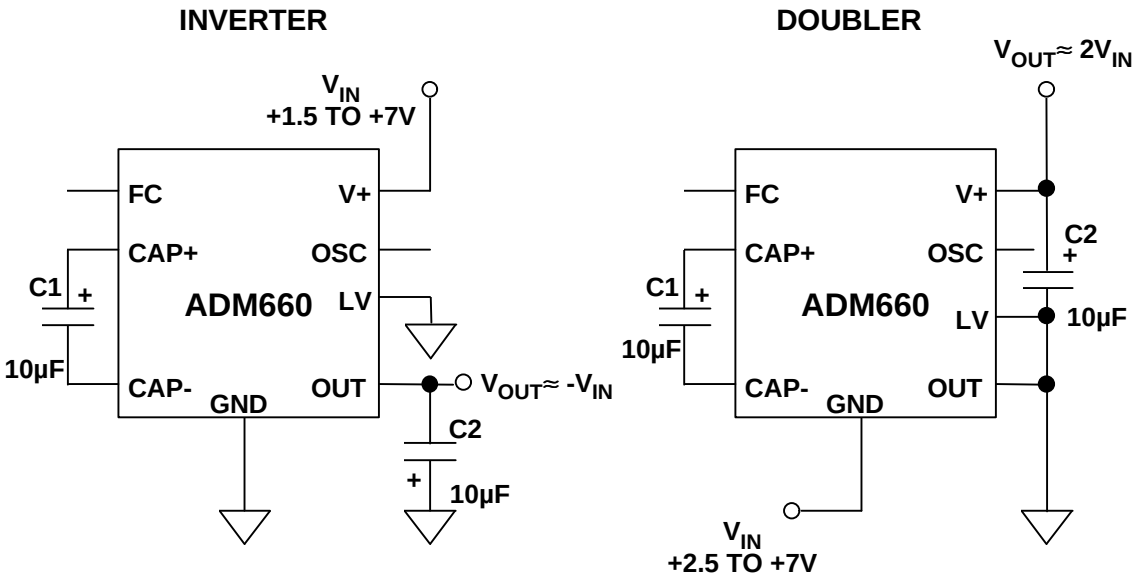


Figure 4.14

ADM660 / ADM8660 KEY SPECIFICATIONS

- **ADM660: Inverts or Doubles Input Supply Voltage**
- **ADM8660: Inverts Input Supply Voltage**
- **Input Range Inverting: +1.5V to +7V**
- **Input Range Doubling: +2.5 to +7V (ADM660)**
- **100mA Output Current**
- **Selectable Switching Frequency: 120kHz or 25kHz**
- **2.2µF or 10µF External Capacitors (120kHz / 25kHz)**
- **600µA Quiescent Current**
- **Shutdown Function (ADM8660), 5µA Shutdown Current**
- **500µs Shutdown Recovery Time**
- **8-Pin SOIC**

Figure 4.15

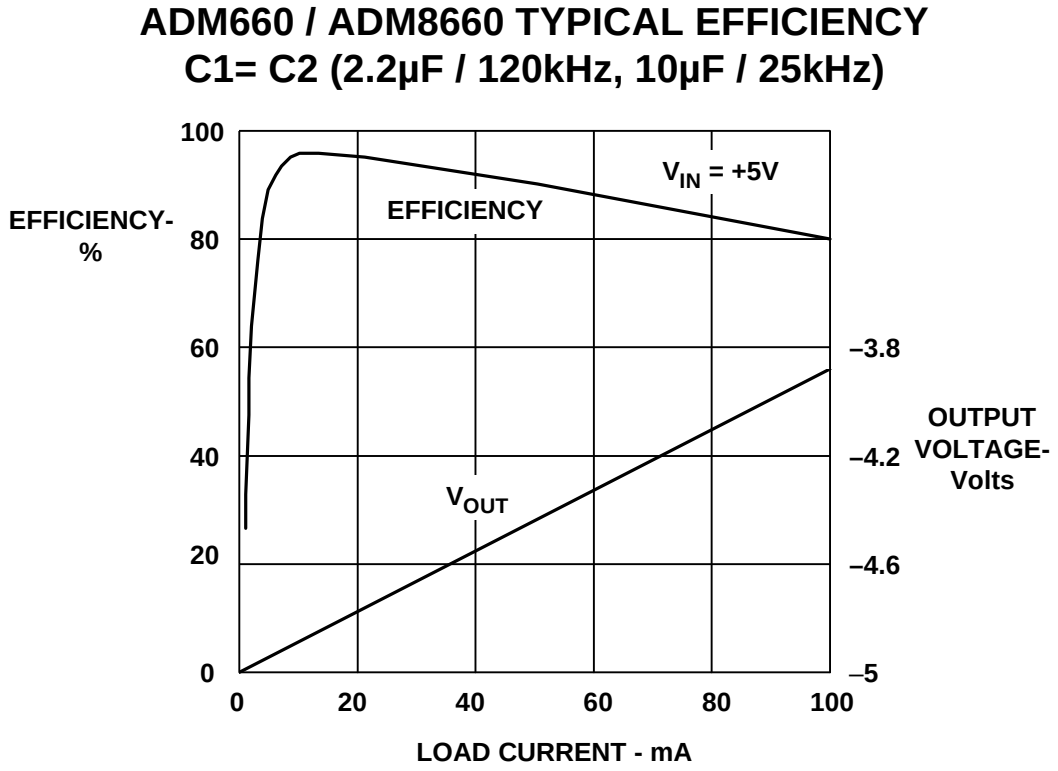


Figure 4.16

REGULATED OUTPUT SWITCHED CAPACITOR VOLTAGE CONVERTERS

Adding regulation to the simple switched capacitor voltage converter greatly enhances its usefulness in many applications. There are three general techniques for adding regulation to a switched capacitor converter. The most straightforward is to follow the switched capacitor inverter/doubler with a low dropout (LDO) linear regulator. The LDO provides the regulated output and also reduces the ripple of the switched capacitor converter. This approach, however, adds complexity and reduces the available output voltage by the dropout voltage of the LDO.

Another approach to regulation is to vary the duty cycle of the switch control signal with the output of an error amplifier which compares the output voltage with a reference. This technique is similar to that used in inductor-based switching regulators and requires the addition of a PWM and appropriate control circuitry. However, this approach is highly nonlinear and requires long time constants (i.e., lossy components) in order to maintain good regulation control.

By far the simplest and most effective method for achieving regulation in a switched capacitor voltage converter is to use an error amplifier to control the on-resistance of one of the switches as shown in Figure 4.17, a block diagram of the ADP3603/3604/3605 voltage inverters. These devices offer a regulated –3V output for an input voltage of +4.5V to +6V. The output is sensed and fed back into the device via the V_{SENSE} pin. Output regulation is accomplished by varying the on-resistance of one of the MOSFET switches as shown by control signal labeled "R_{ON} CONTROL" in the diagram. This signal accomplishes the switching of the MOSFET as well as controlling the on-resistance.

Key features of the ADP3603/3604/3605 series are shown in Figure 4.18. Note that the output regulation of the ADP3605 is ±2%, and the switching frequency is 250kHz. All three devices have a shutdown feature and a turn-on, turn-off time of about 5ms.

A typical application circuit for the ADP3603/3604/3605 series is shown in Figure 4.19. In the normal mode of operation, the SHUTDOWN pin should be connected to ground. The 10µF capacitors should have ESRs of less than 150mΩ, and values of 4.7µF can be used at the expense of slightly higher output ripple voltage. The equations for ripple voltage shown in Figure 4.10 also apply to the ADP3603/3604/3605. Using the values shown, typical ripple voltage ranges from 25mV to 60mV as the output current varies over its allowable range.

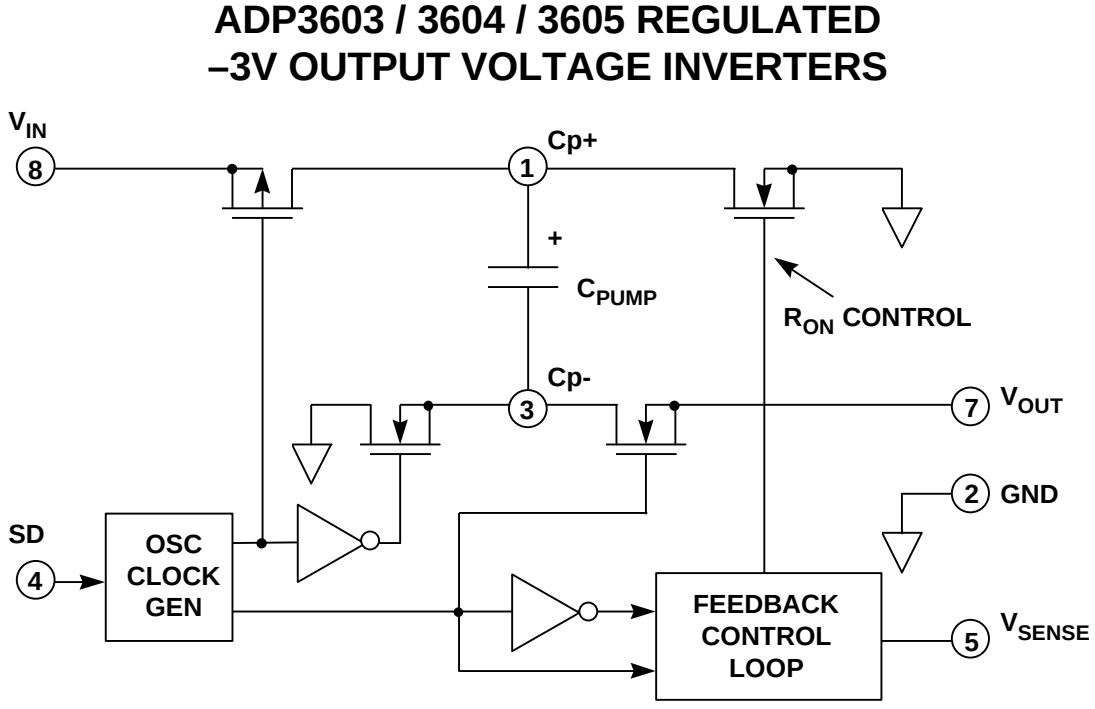


Figure 4.17

ADP3603 / ADP3604 / ADP3605 REGULATED INVERTERS - KEY SPECIFICATIONS

	ADP3603 / 3604	ADP3605
Output Accuracy	±3%	±2%
Switching Frequency	120kHz	250kHz
Turn-On, Turn-Off Time	5ms	5ms
Shutdown Current	1.4mA	10µA
Output Current	50mA / 120mA	120mA
Quiescent Current	2.4mA	2mA
Input Voltage	4.5V to 6V	4.5V to 6V
Nominal Output	–3V	–3V
Package	SO-8	SO-8

Figure 4.18

ADP3603 / 3604 / 3605 APPLICATION CIRCUIT FOR –3V OUTPUT

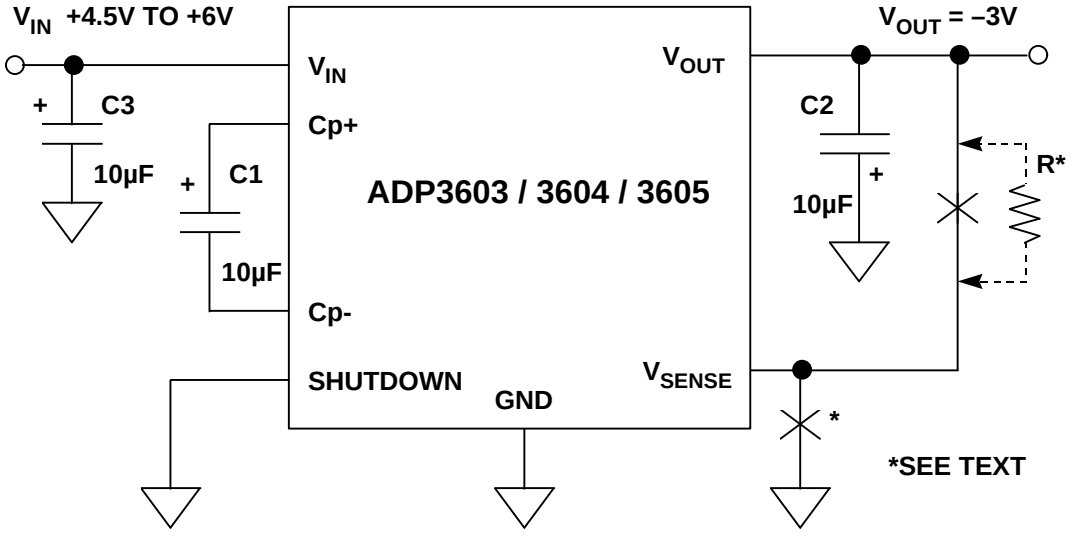


Figure 4.19

The regulated output voltage of the ADP3603/3604/3605 series can varied between –3V and $-V_{IN}$ by connecting a resistor between the output and the V_{SENSE} pin as shown in the diagram. Regulation will be maintained for output currents up to about 30mA. The value of the resistor is calculated from the following equation:

$$V_{OUT} = -\left(\frac{R}{5k\Omega} + 3V\right).$$

The devices can be made to operate as standard inverters providing an unregulated output voltage if the V_{SENSE} pin is simply connected to ground.

The ADP3607/ADP3607-5 are boost switched capacitor voltage regulators based on a regulated voltage doubling topology. The ADP3607-5 is optimized for an output voltage of +5V for inputs between +3V and +5V. The ADP3607 output is adjustable with an external resistor. A block diagram is shown in Figure 4.20 and key specifications in Figure 4.21. The device uses a feedback control scheme similar to the ADP3603/3604/3605 to maintain output voltage regulation for $V_{OUT} < 2V_{IN}$.

ADP3607 SWITCHED CAPACITOR BOOST REGULATOR

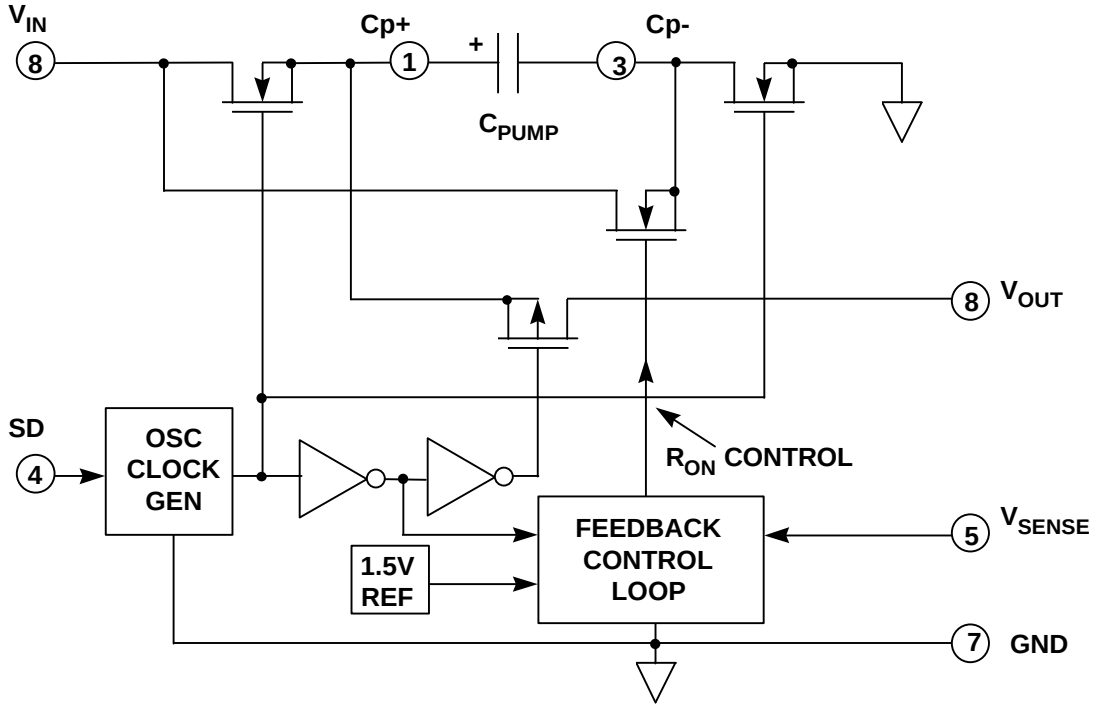


Figure 4.20

ADP3607/ADP3607-5 BOOST REGULATOR KEY SPECIFICATIONS

- **Input Voltage Range: +3V to +5V**
- **Output Voltage: +5V (ADP3607-5)**
- **Adjustable Output Voltage (ADP3607), $V_{OUT} < 2V_{IN}$**
- **Output Current: 50mA**
- **Accuracy: ± 2%**
- **Switching Frequency: 250kHz**
- **Quiescent Current: 2mA**
- **Shutdown Current: 10µA**
- **Turn-On, Turn-Off Time: 50µs**
- **Package: 8-Pin SOIC**

Figure 4.21

A typical application circuit is shown in Figure 4.22. The Schottky diode connecting the input to the output is required for proper operation during start-up and shutdown. If V_{SENSE} is connected to ground, the devices operate as unregulated voltage doublers.

The output voltage of each device can be adjusted with an external resistor. The equation which relates output voltage to the resistor value for the ADP3607 is given by:

$$V_{OUT} = \frac{R}{9.5k\Omega} + 1V, \text{ for } V_{OUT} < 2V_{IN}.$$

The ADP3607 should be operated with an output voltage of at least 3V in order to maintain regulation.

Although the ADP3607-5 is optimized for an output voltage of 5V, its output voltage can be adjusted between 5V and $2V_{IN}$ with an external resistor using the equation:

$$V_{OUT} = \frac{2R}{9.5k\Omega} + 5V, \text{ for } V_{OUT} < 2V_{IN}.$$

ADP3607/ADP3607-5 APPLICATION CIRCUIT

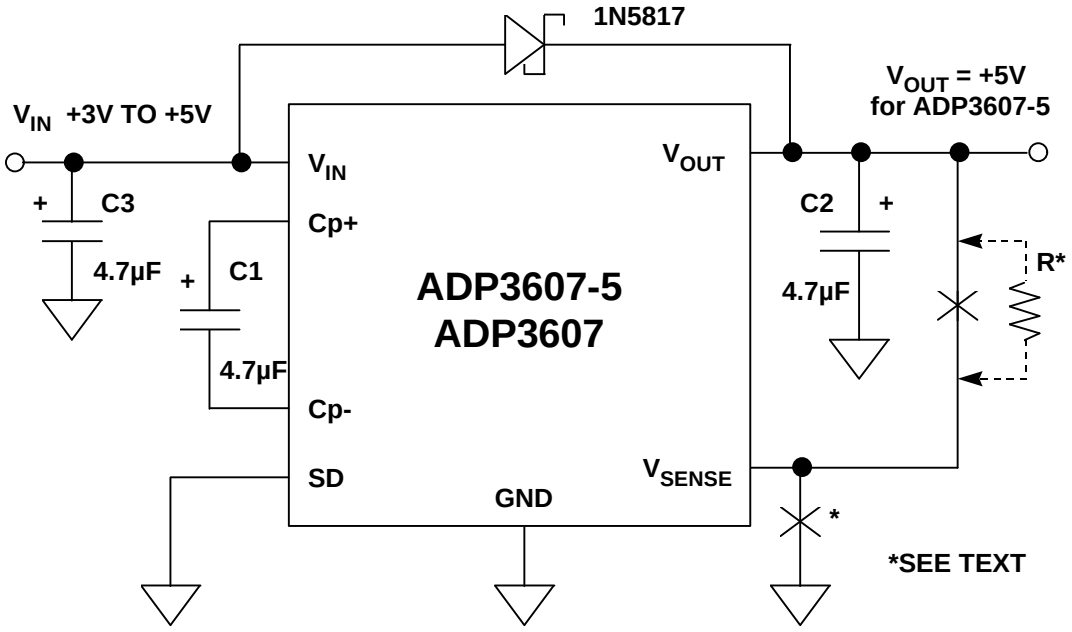


Figure 4.22

When using either the ADP3607 or the ADP3607-5 in the adjustable mode, the output current should be no greater than 30mA in order to maintain good regulation.

The circuit shown in Figure 4.23 generates a regulated 12V output from a 5V input using the ADP3607-5 in a voltage tripler application. Operation is as follows. First assume that the V_{SENSE} pin of the ADP3607-5 is grounded and that the resistor R is not connected. The output of the ADP3607-5 is an unregulated voltage equal to $2V_{IN}$. The voltage at the Cp+ pin of the ADP3607-5 is a square wave with a minimum value of V_{IN} and a maximum value of $2V_{IN}$. When the voltage at Cp+ is V_{IN}, capacitor C2 is charged to V_{IN} (less the D1 diode drop) from V_{OUT1} via diode D1. When the voltage at Cp+ is $2V_{IN}$, the output capacitor C4 is charged to a voltage $3V_{IN}$ (less the diode drops of D1 and D2). The final unregulated output voltage of the circuit, V_{OUT2}, is therefore approximately $3V_{IN} - 2V_D$, where V_D is the Schottky diode voltage drop.

The addition of the feedback resistor, R, ensures that the output is regulated for values of V_{OUT2} between $2V_{IN} - 2V_D$ and $3V_{IN} - 2V_D$. Choosing R = 33.2kΩ yields an output voltage V_{OUT2} of +12V for a nominal input voltage of +5V. Regulation is maintained for output currents up to approximately 20mA.

REGULATED +12V FROM A +5V INPUT USING THE ADP3607-5

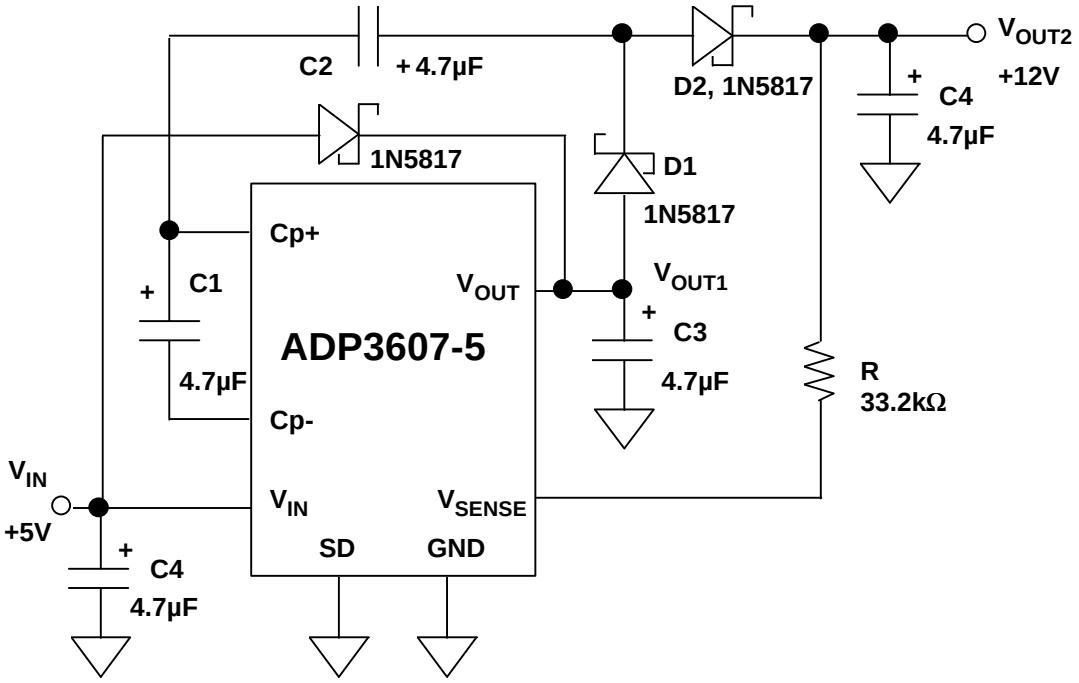


Figure 4.23