Basic DAC Architectures III: Segmented DACs

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SEGMENTED DACS

When we are required to design a DAC with a specific performance, it may well be that no single architecture is ideal. In such cases, two or more DACs may be combined in a single higher resolution DAC to give the required performance. These DACs may be of the same type or of different types and need not each have the same resolution.

In principle, one DAC handles the MSBs, another handles the LSBs, and their outputs are added in some way. The process is known as "segmentation," and these more complex structures are called "segmented DACs". There are many different types of segmented DACs and some, but by no means all, of them will be illustrated in this tutorial.

Figure 1 shows two varieties of segmented voltage-output DAC. The architecture in Figure 1A is sometimes called a Kelvin-Varley Divider and is composed of two or more "string DACs." Since there are buffers between the first and second stages, the second string DAC does not load the first, and the resistors in this string do not need to have the same value as the resistors in the other one. All the resistors in each string, however, do need to be equal to each other or the DAC will not be linear. The examples shown have 3-bit first and second stages but for the sake of generality, let us refer to the first (MSB) stage resolution as M-bits and the second (LSB) as K-bits for a total of $N = M + K$ bits. The MSB DAC has a string of 2^M equal resistors, and a string of 2^K equal resistors in the LSB DAC.
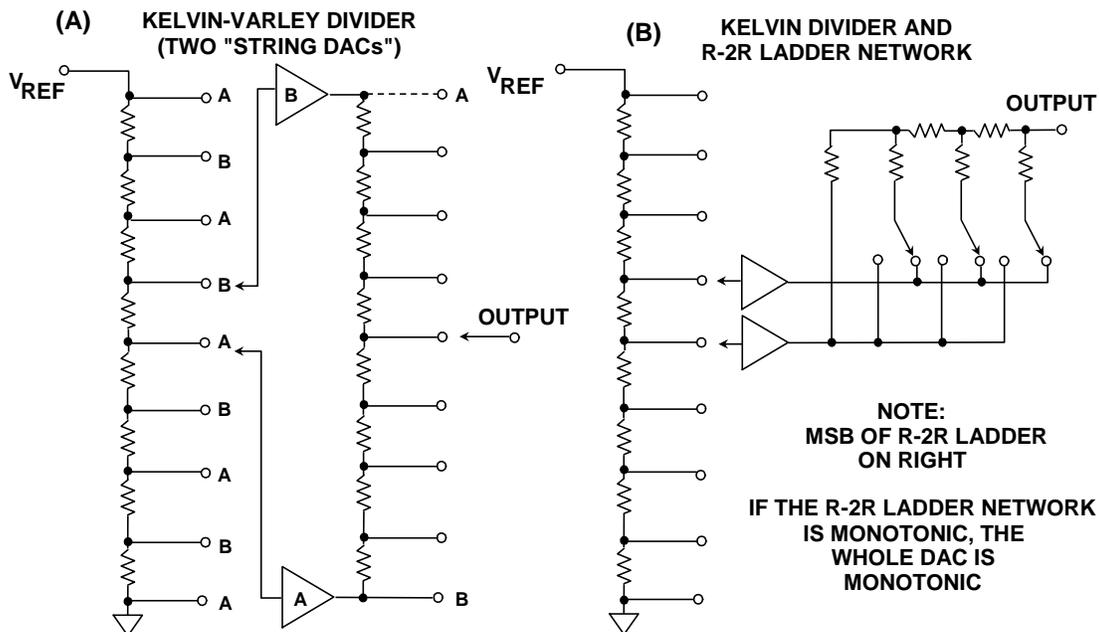
Figure 1: Segmented Voltage-Output DACs

Buffer amplifiers have offset, of course, and this can cause non-monotonicity in a buffered segmented string DAC. In the simpler configuration of a buffered Kelvin-Varley divider buffer (Figure 1A), buffer A is always "below" (at a lower potential than) buffer B, and the extra tap labeled "A" on the LSB string DAC is not necessary. The data decoding is just two priority encoders. In this configuration, however, buffer offset can cause non-monotonicity.

But if the decoding of the MSB string DAC is made more complex so that buffer A can only be connected to the taps labeled "A" in the MSB string DAC, and buffer B to the taps labeled "B," then it is not possible for buffer offsets to cause non-monotonicity. Of course, the LSB string DAC decoding must change direction each time one buffer "leapfrogs" the other, and taps A and B on the LSB string DAC are alternately not used—but this involves a fairly trivial increase in logic complexity and is justified by the increased performance.

Rather than using a second string of resistors, a binary DAC can be used to generate the three LSBs as shown in Figure 1B. It is quite hard to manufacture very high resolution R-2R ladder networks—to be more accurate, it is hard to trim them to monotonicity. So it is quite common to make high resolution DACs with a ladder network for the LSBs, and some other structure for two to five of the MSBs. This voltage-output DAC (Figure 1B) consists of a 3-bit string DAC followed by a 3-bit buffered voltage-mode ladder network.

Dennis Dempsey and Christopher Gorman, "Digital-to-Analog Converter," U.S. Patent 5,969,657, filed July 27, 1997, issued October 19, 1999.
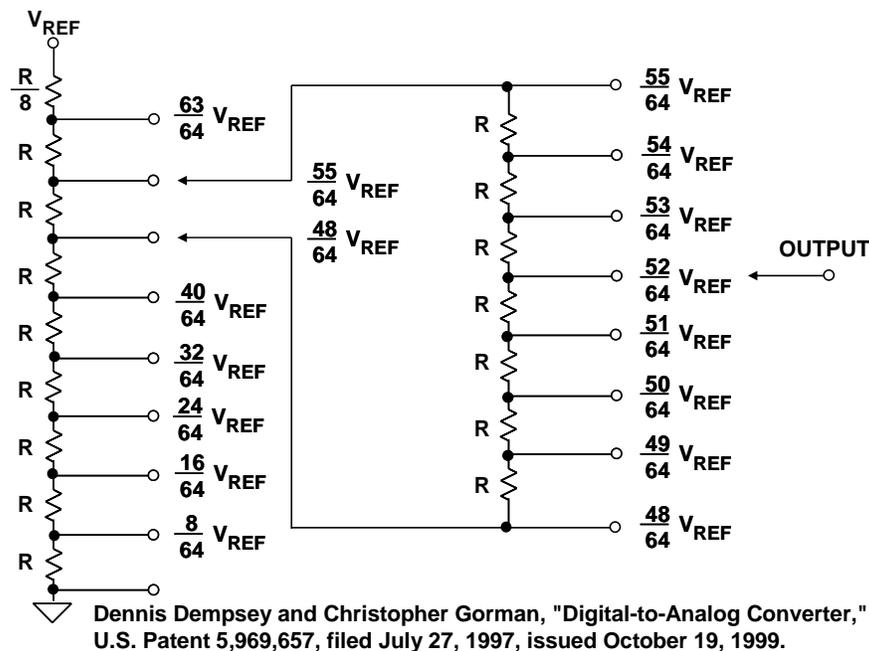
Figure 2: Segmented Unbuffered String DACs Use Patented Architecture

An unbuffered version of the segmented string DAC architecture is shown in Figure 2. This version is more clever in concept (and, of course, can be manufactured on CMOS processes which make resistors and switches but not amplifiers, so it may be cheaper as well). It is intrinsically monotonic.

Here, the resistors in the two strings must be equal, except that the top resistor in the MSB string must be smaller ($1/2^K$ of the value of the others), and the LSB string has $2^K – 1$ resistors rather than 2^K. Because there are no buffers, the LSB string appears in parallel with the resistor in the MSB string that it is switched across and loads it. This drops the voltage across that MSB resistor by 1 LSB of the LSB DAC—which is exactly what is required. The output impedance of this DAC, being unbuffered, varies with changing digital code.

In order to understand this clever concept better, the actual voltages at each of the taps has been worked out and labeled for the 6-bit segmented DAC composed of two 3-bit string DACs shown in Figure 2. The reader is urged to go through this simple analysis with the second string DAC connected across any other resistor in the first string DAC and verify the numbers. A detailed mathematical analysis of the unbuffered segmented string DAC can be found in the relevant patent filed by Dennis Dempsey and Christopher Gorman of Analog Devices in 1997 (Reference 1).

Very high speed DACs for video, communications, and other HF reconstruction applications are often built with arrays of fully decoded current sources. The two or three LSBs may use binary-weighted current sources. It is extremely important that such DACs have low distortion at high frequency, and there are several important issues to be considered in their design.

First of all, currents are never turned on and off—they are steered to one place or another. Turning a current off at high speed frequently involves inductive spikes and, in general, because of capacitance charging, it takes longer than current steering.

Secondly, it is important that the voltage change on the chip required to switch the current should be kept as small as possible. A voltage change causes more charge to flow in stray capacitances and a larger charge-coupled glitch.

Finally, the decoding must be done before the new data is applied to the DAC so that all the data is ready and can be applied simultaneously to all the switches in the DAC. This is generally implemented by using separate parallel latches for the individual switches in a fully decoded array. If all switches were to change state instantaneously and simultaneously there would be no skew glitch—by very careful design of propagation delays around the chip and time constants of switch resistance and stray capacitance the update synchronization can be made very good, and hence the glitch-related distortion is very small.

Two examples of segmented current-output DAC structures are shown in Figure 3. Figure 3A shows a resistor-based approach for the 7-bit DAC where the 3 MSBs are fully decoded, and the 4 LSBs are derived from an R-2R network. Figure 3B shows a similar implementation using current sources. The current source implementation is by far the most popular for today's high-speed reconstruction DACs.
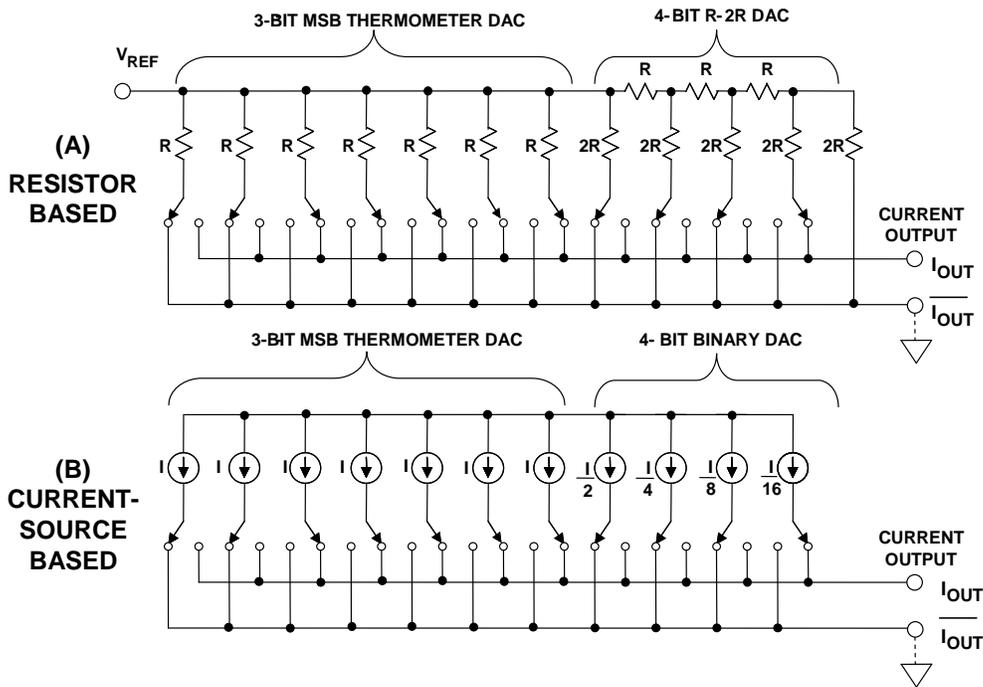
Figure 3: Segmented Current-Output DACs:
(A) Resistor-Based, (B) Current-Source Based

It is also often desirable to utilize more than one fully-decoded thermometer section to make up the total DAC. Figure 4 shows a 6-bit DAC constructed from two fully-decoded 3-bit DACs. As previously discussed, these current switches must be driven simultaneously from parallel latches in order to minimize the output glitch.
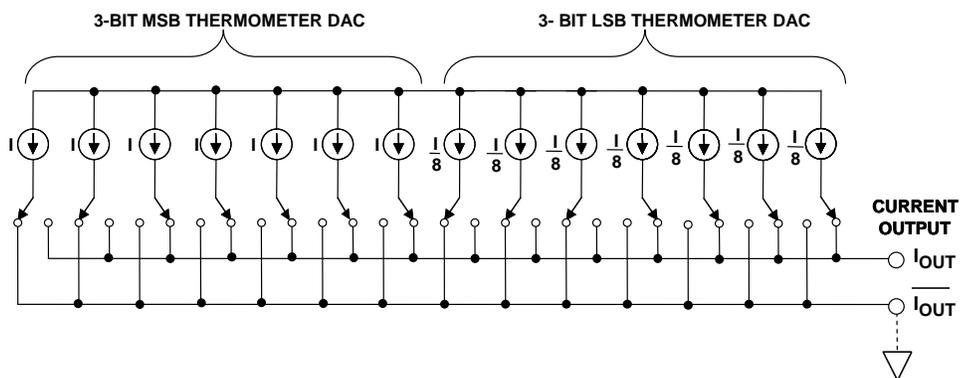
Figure 4: 6-Bit Current-Output Segmented DAC
Based on Two 3-Bit Thermometer DACs

The AD9775 14-bit, 160-MSPS (input)/400-MSPS (output) TxDAC® uses three sections of segmentation as shown in Figure 5. Other members of the AD977x-family and the AD985x-family also use this same basic core.
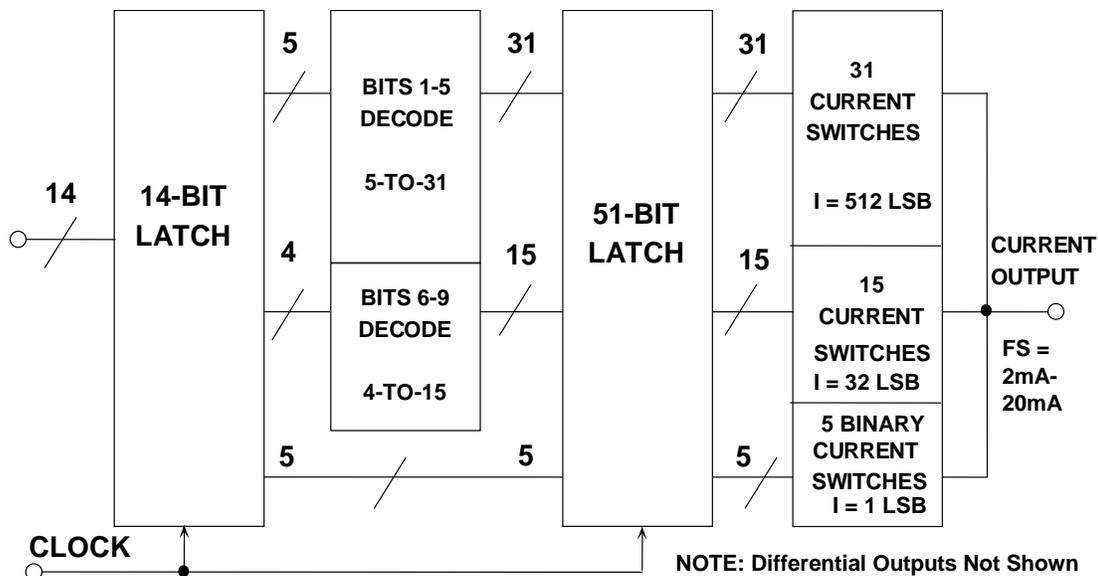
Figure 5: AD9775 TxDAC® 14-Bit CMOS DAC Core

The first 5 bits (MSBs) are fully decoded and drive 31 equally weighted current switches, each supplying 512 LSBs of current. The next 4 bits are decoded into 15 lines which drive 15 current switches, each supplying 32 LSBs of current. The 5 LSBs are latched and drive a traditional binary-weighted DAC which supplies 1 LSB per output level. A total of 51 current switches and latches are required to implement this ultra low glitch architecture.

The basic current switching cell in the TxDAC family is made up of a differential PMOS transistor pair as shown in Figure 6. The differential pairs are driven with low-level logic to minimize switching transients and time skew. The DAC outputs are symmetrical differential currents, which help to minimize even-order distortion products (especially when driving a differential output such as a transformer or an op amp differential current-to-voltage converter).

The overall architecture of the AD977x TxDAC® family and the AD985x-DDS family is an excellent tradeoff between power/performance, and allows the entire DAC function to be implemented on a standard CMOS process with no thin-film resistors.
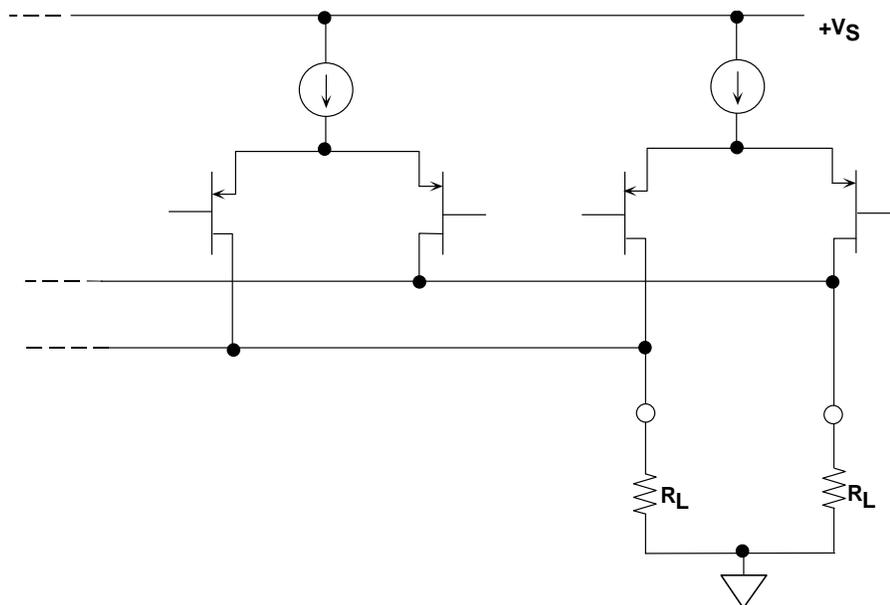
Figure 6: PMOS Transistor Current Switches

REFERENCES:

1. Dennis Dempsey and Christopher Gorman, "Digital-to-Analog Converter," *U.S. Patent 5,969,657*, filed July 27, 1997, issued October 19, 1999. *(describes an elegant solution for segmented unbuffered string DACs).*

2. John A. Schoeff, "An Inherently Monotonic 12 Bit DAC," *IEEE Journal of Solid State Circuits*, Vol. SC-14, No. 6, December 1979, pp. 904-911. *(describes one of the first monolithic DACs to use segmentation).*

3. Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN 0-916550-27-3, Chapter 3. Also available as *The Data Conversion Handbook,* Elsevier/Newnes, 2005, ISBN 0-7506-7841-0, Chapter 3.