In-Amp DC Error Sources

The dc and noise specifications for in-amps differ slightly from conventional op amps, so some discussion is required in order to fully understand the error sources.

GAIN-SETTING RESISTOR ERRORS

The gain of an in-amp is usually set by a single resistor. If the resistor is external to the in-amp, its value is either calculated from a formula or chosen from a table on the data sheet, depending on the desired gain. Examples of in-amps using external gain-setting resistors are the AD620, AD623, AD627, AD8220 (JFET input, rail-to-rail output), AD8221, AD8222, AD8223, and AD8224.

Absolute value laser wafer trimming allows the user to program gain accurately with this single resistor. The absolute accuracy and temperature coefficient of this resistor directly affects the in-amp gain accuracy and drift. Since the external resistor will never exactly match the internal thin film resistor tempcos, a low TC (< 25 ppm/°C) metal film resistor should be chosen, preferably with a 0.1% or better accuracy.

Often specified as having a gain range of 1 to 1,000, or 1 to 10,000, many in-amps will work at higher gains, but the manufacturer will not guarantee a specific level of performance at these high gains. In practice, as the gain-setting resistor becomes smaller, any errors due to the resistance of the metal runs and bond wires become significant. These errors, along with an increase in noise and drift, may make higher single-stage gains impractical. In addition, input offset voltages can become quite sizable when reflected to output at high gains. For instance, a 0.5 mV input offset voltage becomes 5 V at the output for a gain of 10,000. For high gains, the best practice is to use an in-amp as a preamplifier, then use a post amplifier for further amplification.

In a *pin-programmable-gain* in-amp such as the AD621, AD624, the gain-set resistors are internal, well matched, and the device gain accuracy and gain drift specifications include their effects. The AD621 is otherwise generally similar to the externally gain-programmed AD620.

The AD8250, AD8251, and AD8253 have *both pin and software programmable* gains and are designed on the Analog Devices' *i*CMOS® process which allows operation on supply voltages from ±5 V to ±15 V. Input impedance of these devices is in the GΩ region.

GAIN ERROR AND GAIN NONLINEARITY

The *gain error* specification is the maximum deviation from the gain equation. Monolithic in-amps such as the AD8221 (BR Grade) have very low factory trimmed gain errors, with its maximum error of 0.02% at G = 1 and 0.15% at G = 1000 for this high quality in-amp. Notice

that the gain error increases with increasing gain. Although externally connected gain networks allow the user to set the gain exactly, the temperature coefficients of the external resistors and the temperature differences between individual resistors within the network all contribute to the overall gain error. If the data is eventually digitized and presented to a digital processor, it may be possible to correct for gain errors by measuring a known reference voltage and then multiplying by a constant.

Gain nonlinearity is defined as the maximum deviation from a straight line on the plot of output versus input. The straight line is drawn between the end-points of the actual transfer function. Gain nonlinearity in a high quality in-amp is usually 0.01% (100 ppm) or less, and is relatively insensitive to gain over the recommended gain range.

INPUT OFFSET VOLTAGE AND BIAS CURRENT ERRORS

The total *input offset voltage* of an in-amp consists of two components (see Figure 1 below). *Input* offset voltage, V_{OSI}, is the input offset component that is reflected to the output of the in-amp by the gain G. *Output* offset voltage, V_{OSO}, is independent of gain.

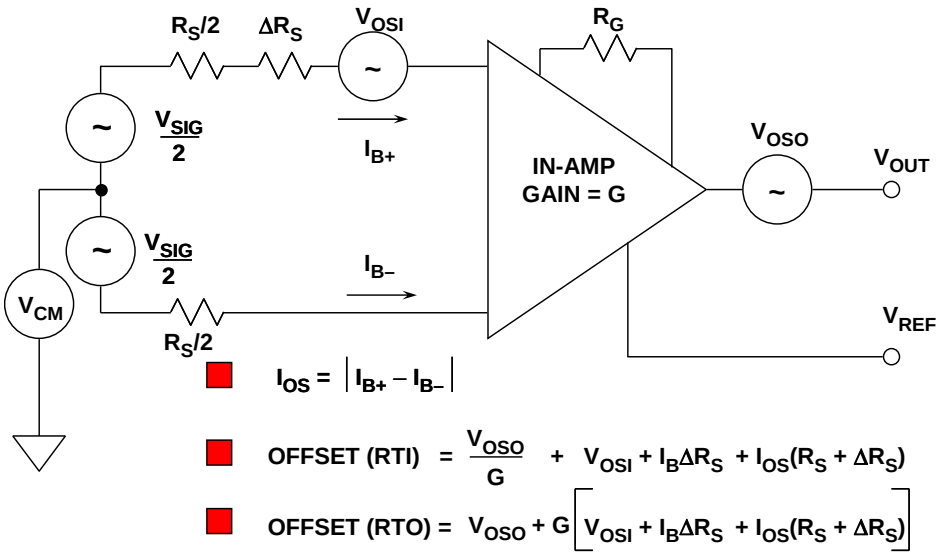

Figure 1: In-Amp Offset Voltage Model

At low gains, output offset voltage is dominant, while at high gains input offset dominates. The output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by a drift specification at a high gain (where output offset effects are negligible).

The total output offset error, referred to the input (RTI), is equal to $V_{OSI} + V_{OSO}/G$. In-amp data sheets may specify V_{OSI} and V_{OSO} separately, or give the total RTI input offset voltage for different values of gain.

Input bias currents may also produce offset errors in in-amp circuits (Fig. 1, again). If the source resistance, R_S, is unbalanced by an amount, ΔR_S, (often the case in bridge circuits), then there is an additional input offset voltage error due to the bias current, equal to $I_B \Delta R_S$ (assuming that $I_{B+} \approx I_{B-} = I_B$). This error is reflected to the output, scaled by the gain G.

The input offset current, I_{OS}, creates an input offset voltage error across the source resistance, $R_S+\Delta R_S$, equal to $I_{OS}(R_S+\Delta R_S)$, which is also reflected to the output by the gain, G.

COMMON-MODE REJECTION AND POWER SUPPLY REJECTION ERRORS

In-amp *common mode error* is a function of both gain and frequency. Analog Devices specifies in-amp CMR for a 1 kΩ source impedance unbalance at a frequency of 60 Hz. The RTI common mode error is obtained by dividing the common mode voltage, V_{CM}, by the common mode rejection ratio, CMRR.

Figure 2 below shows the CMR for the AD620 in-amp as a function of frequency, with a 1 kΩ source impedance imbalance.

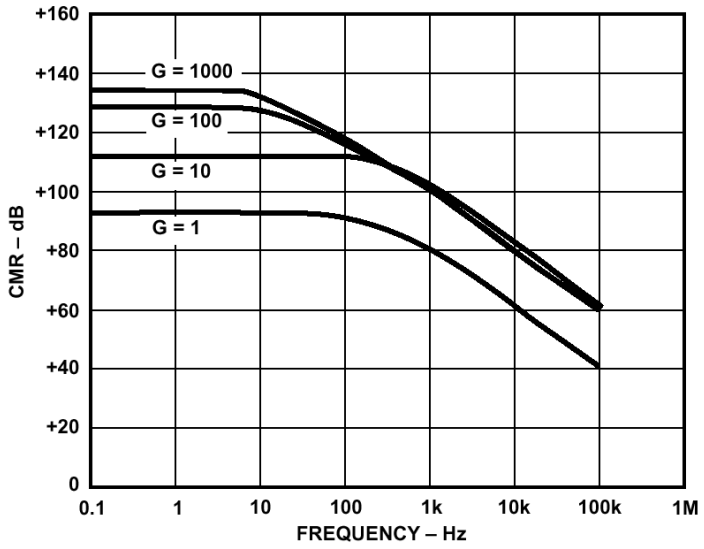

Figure 2: AD620 In-Amp Common-Mode Rejection (CMR) Versus Frequency For 1 kΩ Source Imbalance

Power supply rejection (PSR) is also a function of gain and frequency. For in-amps, it is customary to specify the sensitivity to each power supply separately, as shown in Figure 3 below for the AD620. The RTI power supply rejection error is obtained by dividing the power supply deviation from nominal by the power supply rejection ratio, PSRR.

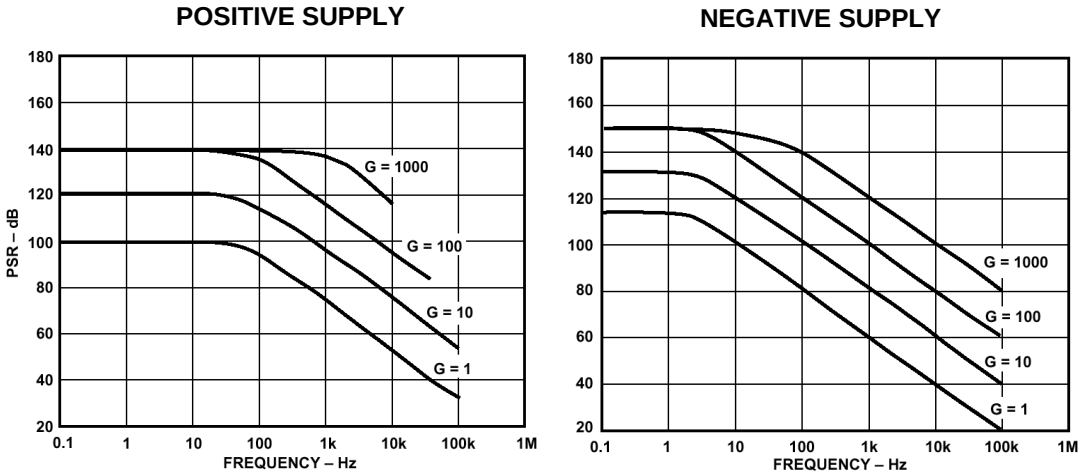

Figure 3: AD620 In-Amp Power Supply Rejection (PSR) Versus Frequency

Because of the relatively poor PSR at high frequencies, decoupling capacitors are required on both power pins to an in-amp. Low inductance ceramic capacitors (0.01 to 0.1 µF) are appropriate for high frequencies. Low ESR electrolytic capacitors should also be located at several points on the PC board for low frequency decoupling.

TOTAL IN-AMP DC ERROR BUDGET

Now that all dc error sources have been accounted for, a worst case dc error budget can be calculated by reflecting all the sources to the in-amp input, as is illustrated by the table of Figure 4, below.

ERROR SOURCE	RTI VALUE
Gain Accuracy (ppm)	Gain Accuracy × FS Input
Gain Nonlinearity (ppm)	Gain Nonlinearity × FS Input
Input Offset Voltage, V_{OSI}	V_{OSI}
Output Offset Voltage, V_{OSO}	$V_{OSO} \div G$
Input Bias Current, I_B, Flowing in ΔR_S	$I_B \Delta R_S$
Input Offset Current, I_{OS}, Flowing in R_S	$I_{OS}(R_S + \Delta R_S)$
Common Mode Input Voltage, V_{CM}	$V_{CM} \div$ CMRR
Power Supply Variation, ΔV_S	$\Delta V_S \div$ PSRR

Figure 4: In-Amp DC Errors Referred to the Input (RTI)

It should be noted that the dc errors can be referred to the in-amp output (RTO), by simply multiplying the RTI error by the in-amp gain.

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